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Novel quadrature voltage controlled oscillator using series transistors coupling

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In this paper, a novel quadrature voltage controlled oscillator (QVCO) coupled by four transistors has been presented. The proposed QVCO consists of two identical LC negative resistance voltage controlled oscillators (VCO) and four series coupling transistors. Compared with the coupling method using paralleled transistors, the series transistors coupling method has lower power consumption and phase noise. The proposed QVCO is designed and simulated with Global Foundries 0.18 μm CMOS 1P6M RF process using Cadence IC Design Tools. The simulation results demonstrate that the proposed QVCO operates from 2.388 GHz to 3.376 GHz by adjusting the control voltage, and its phase noise is –140.6 dBc/Hz at 1 MHz offset. Moreover, the power consumption of the QVCO is only 1.84 mW with 1.25 V supply voltage.

Keywords: CMOS, Radio frequency (RF), Negative resistance, Phase noise, Quadrature voltage controlled oscillator

1 Introduction

With the rapidly development of wireless communication technology and microelectronics process, greater demand of low power and highly integrated radio frequency integrated circuits (RFIC) becomes more and more urgent. As one of the most important building block of the wireless transceivers, the VCO provides local oscillation signal for the mixer to realize the spectrum shifting of the useful signals. The super-heterodyne transceiver and direct conversion transceiver are the two most important architectures in modern wireless transceiver systems. However, the structure of the super-heterodyne transceiver is very complex, and it suffers from serious image frequency interference. Moreover, the super-heterodyne transceiver requires expensive and large chip area filters, which increases its cost. The direct conversion transceivers[1] become more and more popular because of their simplicity, low power consumption and unnecessary of expensive and large chip area filters. Figure 1 is the block diagram of a direct conversion transceiver. As it is shown in Fig. 1, its structure is very simple, and the QVCOs are critical building blocks of the direct conversion transceiver. There are four main methods to generate quadrature sinusoidal signals: using a polyphase filter converts the differential signal into four quadrature signals[2] using a phase-locked loop (PLL) and a frequency divider to generate quadrature signals[3-7] the current-mode approach using active integrator[8-13] using two identical VCOs coupled by transistors or transformers to generate quadrature signals[14]. However, the polyphase filter method will attenuate the signals, and the amplitudes of the output quadrature signals are relatively small. The PLL and frequency divider method requires a large number of flip-flops, complex structure and higher power consumption is inevitable. The current-mode quadrature oscillators are very popular in low frequency applications, and they are very easy to be implemented. However, the applications of current-mode quadrature oscillators are limited by their lower oscillation frequencies. The QVCOs based on the coupling method using transformers or transistors have the advantages of lower phase noise, lower power consumption and accurate quadrature outputs, and they are widely used in direct conversion transceivers. A novel QVCO coupled by four transistors is demonstrated in this paper. The proposed QVCO is based on two identical negative resistance *LC* oscillators, and they are coupled with four P&N transistors. The cadence IC design tools simulation results show that the oscillation frequency of the QVCO can be tuned from 2.388 GHz to 3.376 GHz by adjusting the control voltage, and its power consumption is only 1.84 mW. The proposed QVCO has the

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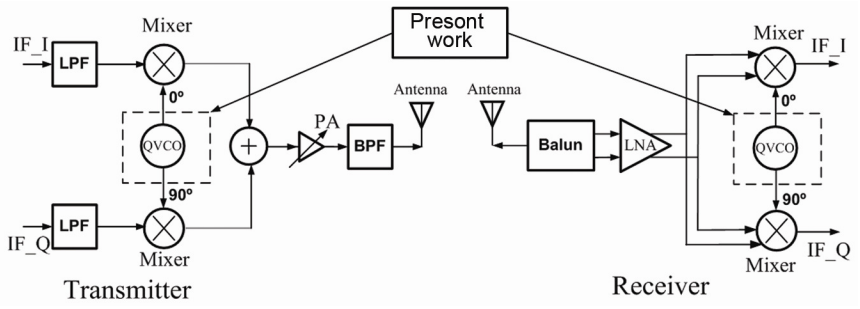

Fig. 1—Block diagram of direct conversion transceiver

characteristics of low power and simple structure, and it is suitable for wireless communication applications.

2 Circuit Analyses

2.1 Negative resistance *LC* oscillator

An LC oscillator could be considered as an interconnection of a passive *LC* tank and an active negative resistance. Figure 2(a) is an analogy of LC tank VCO[15]. The paralleled passive LC tank is a frequency selective network, and the active negative resistance is used for energy compensation of the paralleled passive LC tank.

Assuming that there is a pulse current $i(t)=I_{pulse}\,\delta(t)$ applied to the passive LC tank, and the response in time domain of the tank could be expressed as:

$$v_{out}(t) \approx \frac{I_{pulse} e^{\frac{-t}{2RC}}}{C}\left(\sqrt{\left(\frac{1}{LC}-\frac{1}{4R^2C^2}\right)}t\right) \quad \ldots (1)$$

From Eq. (1), it is clear that the output of the passive LC tank is a sinusoidal signal, and the amplitude decay of the sinusoidal signal is inversely proportional to the capacitor of the tank. When $R^2 >> (L/C)$, and the frequency of the output sinusoidal signal could be expressed as:

$$f_{osc} = \frac{1}{2\pi}\sqrt{\frac{1}{LC}} \quad \ldots (2)$$

Then, to keep the output sinusoidal signal in a steady state with constant amplitude, the energy loss is compensated by the active negative resistance.

2.2 LC oscillator

The schematic of the LC oscillator is presented in Fig. 2(b). The presented LC oscillator consists of two transistors (one NMOS transistors and one PMOS transistors) and a LC frequency selective tank.

Figure 3 is the AC equivalent circuit of the LC oscillator. Looking into the terminals A and B, we

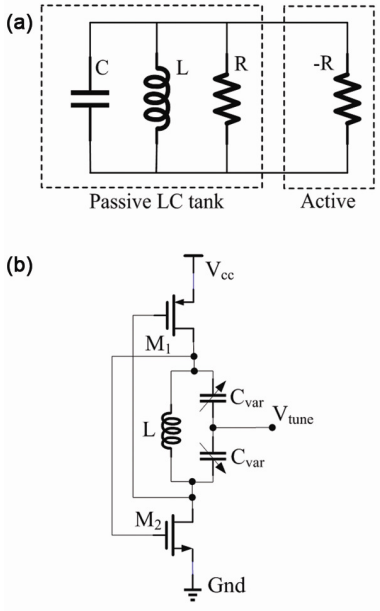

Fig. 2—(a) Analogy of LC VCO (b) LC oscillator

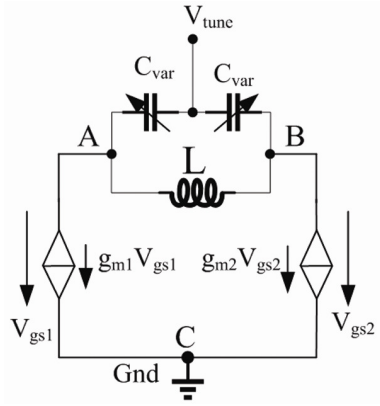

Fig. 3—AC equivalent circuit of the LC oscillator

may notice that the transistors M_1 and M_2 consist of a single-port network, respectively. Assuming that the characteristics of the two transistors are identical, this means:

$$g_{m1} = g_{m2} \quad \ldots (3)$$

From Figs 2(b) and 3, we can know that:

$$\begin{cases} v_{gs1} = v_{ds2} \\ v_{gs2} = v_{ds1} \end{cases} \quad \ldots (4)$$

When the oscillator operates at steady state, the voltage amplitudes at the terminals A and B are symmetrical and equal, then:

$$v_{ds1} = -v_{ds2} \quad \ldots (5)$$

The AC equivalent conductance between the terminals A and C could be expressed as:

$$G_{AM} = \frac{g_{m1} v_{gs1}}{v_{ds1}} = -g_m \quad \ldots (6)$$

Similarly, the AC equivalent conductance between the terminals B and C is:

$$G_{BM} = \frac{g_{m2} v_{gs2}}{v_{ds2}} = -g_m \quad \ldots (7)$$

The input resistance between the terminals A and B could be expressed as:

$$R_{in(AB)} = -\left(\frac{1}{g_m} + \frac{1}{g_m}\right) = -\frac{2}{g_m} \quad \ldots (8)$$

Based on the above analysis, the simplified AC equivalent circuit of the LC oscillator is presented in Fig. 4. The equivalent circuit in Fig. 4 is a classic LC negative resistance oscillator, and the whole negative resistance of the oscillator is about $-2/g_m$. When the negative resistance $R_{in(AB)}$ equals to the parasitic resistance of the LC parallel resonant tank, the negative resistance provides the energy loss of the LC parallel resonant tank, and the oscillator maintains steady oscillation.

2.3 Proposed transistors coupled QVCO

The schematic of the proposed QVCO is presented in Fig. 5. The proposed QVCO consists of two negative resistance LC oscillators, and they are coupled with each other by using four transistors (M_a, M_b, M_c and M_d). Assuming that the characteristics of $M_1 - M_4$ and $M_a - M_d$ are identical, which means the transconductance of the transistors satisfy Eq. (9):

$$\begin{cases} g_{m1} = g_{m2} = g_{m3} = g_{m4} \\ g_{ma} = g_{mb} = g_{mc} = g_{md} \end{cases} \quad \ldots (9)$$

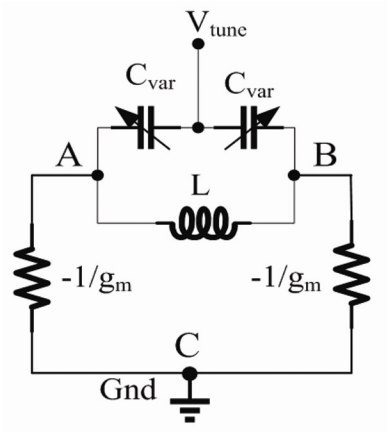

Fig. 4—The simplified AC equivalent circuit of the LC oscillator

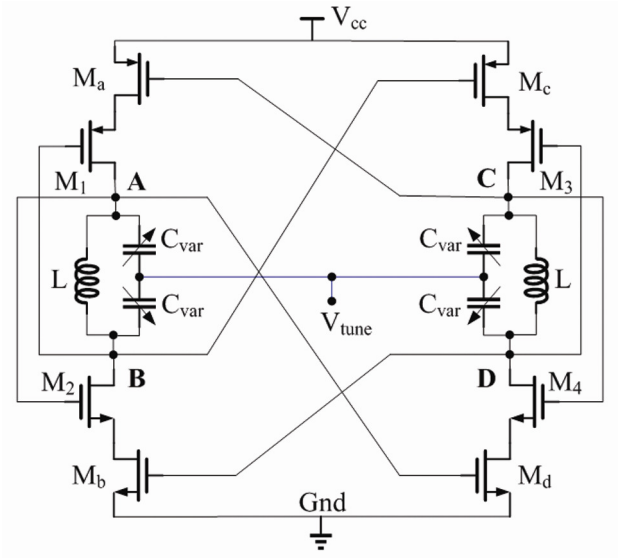

Fig. 5—The proposed QVCO

From Fig. 5, the drain currents of the transistors $M_1 - M_4$ and $M_a - M_d$ could be expressed as:

$$\begin{cases} i_{ds2} = i_{dsb} = g_{mb} v_D \\ i_{ds4} = i_{dsd} = g_{md} v_A \\ i_{ds1} = i_{dsa} = g_{ma} v_C \\ i_{ds3} = i_{dsc} = g_{mc} v_B \end{cases} \quad \ldots (10)$$

The AC voltages of nodes A, B, C and D satisfy Eq. (11):

$$\begin{cases} v_A = v_B + i_{ds2} Z(j\omega) \\ v_C = v_D + i_{ds4} Z(j\omega) \end{cases} \quad \ldots (11)$$

where $Z(j\omega)$ is reactance of the LC tank. Moreover, from the analysis of negative LC oscillator, the AC

signals at nodes A, B and C, D are inverted, respectively. The voltages at nodes A, B and C, D satisfy Eq. (12):

$$\begin{cases} v_A = -v_B \\ v_C = -v_D \end{cases} \quad \ldots (12)$$

Setting Eq. (12) into Eq. (11), Eq. (13) is obtained as:

$$\begin{cases} i_{ds2} = \dfrac{v_A Z(j\omega)}{2} \\ i_{ds4} = \dfrac{v_C Z(j\omega)}{2} \end{cases} \quad \ldots (13)$$

Combining Eqs (10), (12) and (13), Eq. (14) is obtained as:

$$\begin{cases} v_A^2 + v_C^2 = 0 \\ v_B^2 + v_D^2 = 0 \\ v_A = \pm j v_C \\ v_B = \pm j v_D \end{cases} \quad \ldots (14)$$

From Eqs (12) and (14), it is clear that four quadrature signals are generated.

3 Post-Layout Simulation Results

The proposed QVCO is designed and verified by using Cadence IC Design Tools 5.1.41 Spectre simulator with GlobalFoundries' 0.18 µm 1P6M CMOS RF process. The physical chip layout is presented in Fig. 6, and the Mentor Calibre software is used for its DRC, LVS and PEX layout verifications. In order to satisfy the metal density requirements of the chip, some dummy metals have been added. The active chip area including the bond pads of the QVCO is approximately 0.85×0.52 mm^2.

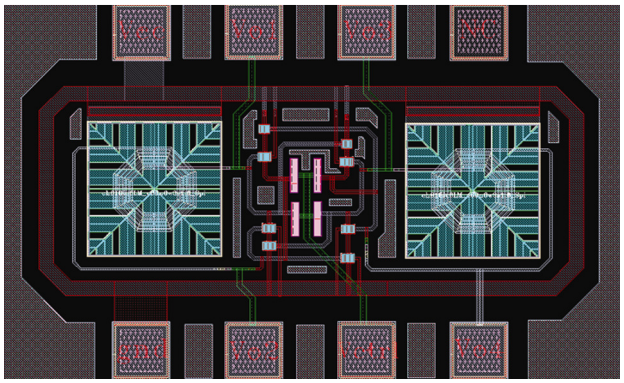

Fig. 6—The physical chip layout of the QVCO (0.85×0.52 mm^2)

After extracting the parasitics and connecting the parasitics to the schematic, the post-layout simulation results of the QVCO are presented in Figs 7-12. Figures 7-10 are the post-layout transient response of the QVCO. Figure 8 is the transient response of the QVCO during its initial state. From Fig. 7, it is clear that the starting time of the QVCO is about 10 ns.

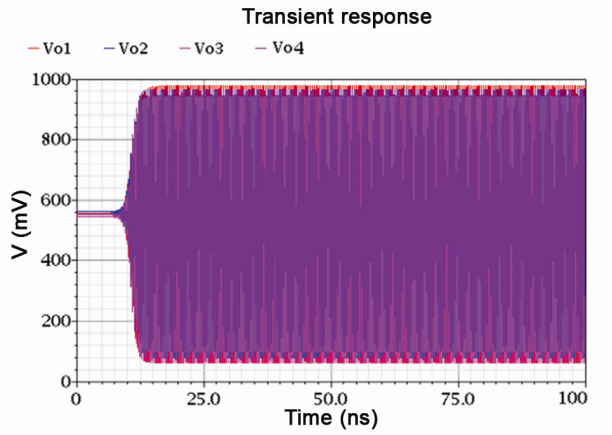

Fig. 7—The transient response of the QVCO

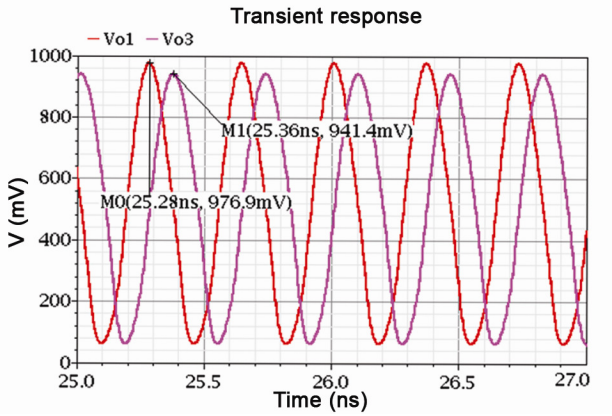

Fig. 8—The simulated V_{o1} and V_{o3} at steady state

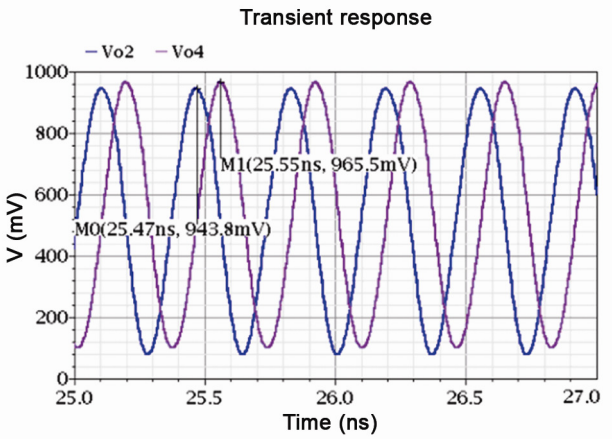

Fig. 9—The simulated V_{o2} and V_{o4} at steady state

Figures 8 and 9 are the simulated V_{o1}, V_{o3} and V_{o2}, V_{o4} at steady state, respectively. Figure10 is the simulated V_{o1}, V_{o2}, V_{o3} and V_{o4} from 25 ns to 27 ns. Figure 11 is the harmonic balance simulation result of V_{o1}. As is shown in Fig. 11, the oscillation frequency of the QVCO is about 2.758 GHz. The output power of the 2.758 GHz signal is about 2.926 dBm, and the other output interference harmonic signals are relatively small. Moreover, from the marks M_0 and M_1 in Fig. 8, it is easy to calculate the phase difference of V_{o1} and V_{o3} is (0.08/0.362)×2π = 89.5°; from the marks M_0 and M_1 in Fig. 9, it is also easy to calculate the phase difference of V_{o2} and V_{o4} is also (0.08/0.362)×2π = 89.5°. From the above analysis, the QVCO provides four quadrature signals, and the phase errors are about 0.55%. Figure 12 is post-layout simulation result of the phase noise of the QVCO. As is shown in Fig. 12, the phase noise of the QVCO is about is –140.6 dBc/Hz at 1 MHz offset. Figure 13 is the post-layout simulation result of the frequency tuning range of the proposed QVCO, the output frequency of the QVCO versus the control voltage is described in Fig. 13. From the markers M_0 and M_1 in Fig. 13, it is clear that when the control voltage (V_{ctrl}) varies from 0 V to 1.3 V, the output frequency of the QVCO could be tuned from 2.388 GHz to 3.376 GHz, its frequency tuning range is about 0.988 GHz. Moreover, the frequency of the QVCO could be approximately linearly adjusted by the control voltage. Table 1 summarizes the recently reported QVCOs along with this work. It is observed that the proposed LC QVCO has the advantages of lower power consumption, better phase noise performance and smaller chip area.

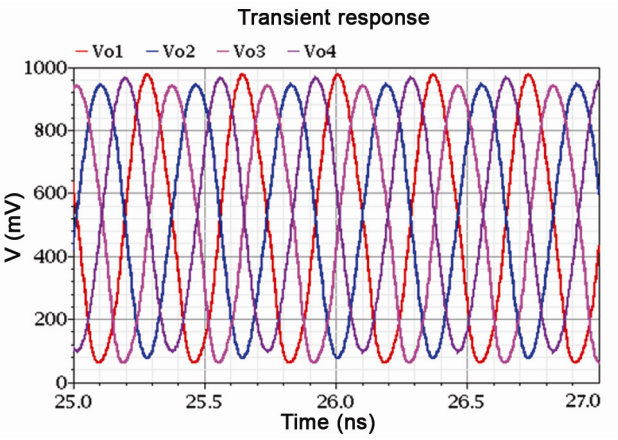

Fig. 10—The simulated V_{o1} - V_{o4} at steady state

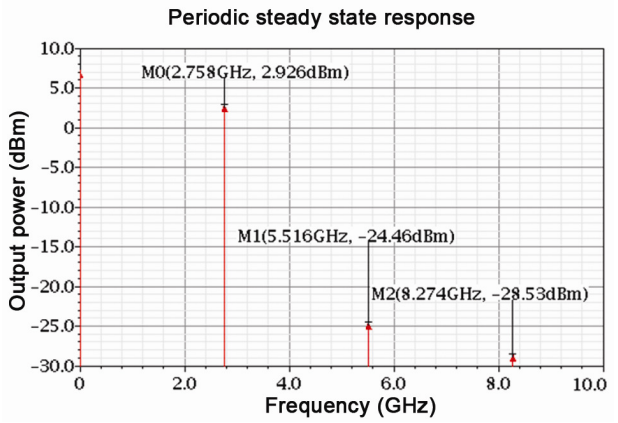

Fig. 11—The harmonic balance simulation result of V_{o1}

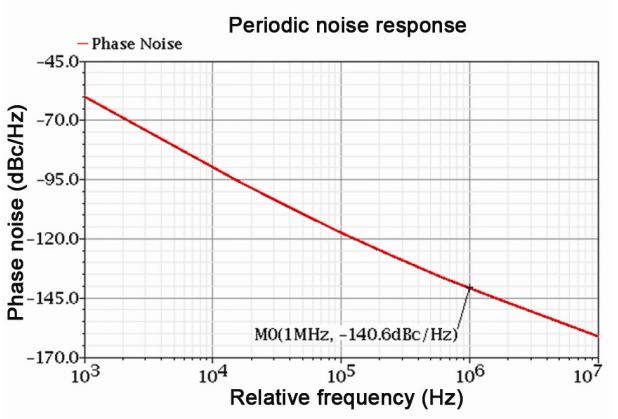

Fig. 12—The phase noise of the QVCO

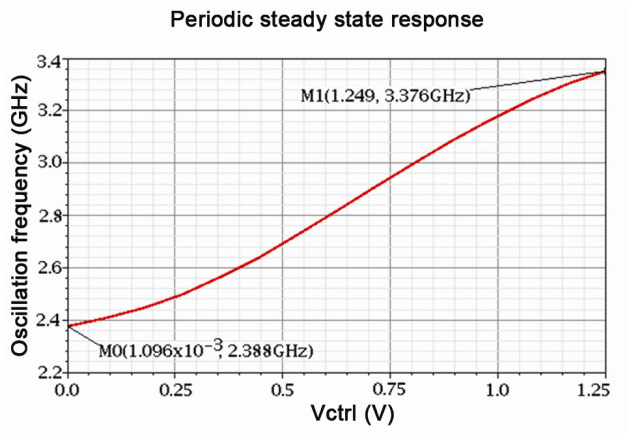

Fig. 13—The frequency tuning range of the QVCO

Table 1—Performance comparison with recently reported QVCOS

References	[16]	[17]	[18]	[19]	Present
Technology (μm)	0.18	0.18	0.18	0.18	0.18
Supply voltage (V)	1.5	1.2	1.1	1.0	1.25
Power consumption (mW)	8.22	3.3	1.92	3.2	1.84
Phase noise (dB)	-125	-123.2	117.1	-114	-140.6
Tuning range (GHz)	1.8	0.74	0.15	0.24	0.988
Chip area (mm^2)	0.63	0.48	0.45	0.58	0.442

4 Conclusions

A novel quadrature QVCO coupled by four P&N transistors is presented in this paper, and the GlobalFoundries' 0.18 μm 1P6M CMOS RF process is used to design and verify the proposed QVCO. The Mentor Calibre software is used for the DRC, LVS and PEX layout verifications of the QVCO. After extracting the parasitics and connecting the parasitics to the schematic, the Cadence post-layout simulation results demonstrate that the power consumption is only 1.84 mW from a 1.25V supply voltage, and the linear frequency tuning range of the QVCO is about 0.988 GHz.

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